

REMARKS

Claims 1, 6-8 and 13-16 are pending in the above-identified application. Claims 2-5 are canceled and non-elected claims 9-12 are canceled. Claims 13-16 are added. Claim 1 is amended.

Claims 1, 2, 4, and 6-8 were rejected under 35 U.S.C. 102(b) as being anticipated by *Lee* (U.S. Patent No. 6,251,737 B1.) Applicants have amended claim 1 to include the features of claims 2 and 3. Accordingly, withdrawal of this rejection is respectfully requested.

This rejection is also improper because the *Lee* reference fails to disclose all claim limitations. For example, *Lee* fails to disclose a sidewall film. The Examiner mischaracterized the silicide layer 132 (e.g., insulation layer) as a sidewall film. However, assuming for argument purposes that the silicide layer 132 is a sidewall film, the silicide layer 132 in *Lee* does not cover a low permittivity region 136 (Fig. 1H). Therefore, *Lee* fails to disclose *a low permittivity region locally provided at a lower portion of the side surface of said gate with the low permittivity region being covered by said sidewall film.*

In view of the above remarks, Applicants respectfully request that dependent claims 6-8 also be allowed.

Claims 1-5 were rejected under 35 U.S.C. 102(b) as being anticipated by *Wu* (U.S. Patent No. 6,180,988 B1.) Withdrawal of this rejection is respectfully requested.

This rejection is improper because the *Wu* reference fails to disclose all claim limitations. For example, *Wu* fails to disclose *a sidewall film contacting a side surface of said gate.* Rather, *Wu* teaches that the “silicon oxynitride layer 10 remains between the gate polysilicon 8 and the

side-wall spacers 12 (page 3, lines 44-46; Fig. 2.) Thus, the silicon oxynitride layer 10 -- not the side-wall spacers 12 -- covers the side surface of the gate.

Also, as shown in Fig. 8 of *Wu*, a silicon oxynitride layer 10 is formed between a gate electrode 8 and a component of spacers 18 and an oxide 26. However, the present invention discloses to form a lower permittivity material or the cavity so as to *directly contact* both sides of a lower portion of the gate (a portion on which an electric field concentrates.)

Claims 1-3 were also rejected under 35 U.S.C. 102(e) as being anticipated by *Scholer et al.* (U.S. Pat. No. 6,433,371 B1.) Withdrawal of this rejection is respectfully requested.

This rejection is improper because the cited reference fails to disclose all claim limitations. For example, *Scholer et al.* fails to disclose a gate electrode that has *a nearly rectangular shaped section*. Rather, in *Sholer et al.*, a shape of a section of the gate is restricted to "trapezoidal". Therefore, in *Sholer et al.*, the manufacturing process is more complicated and difficult and it nearly impossible to form a cavity so as to directly contact both sides of a lower portion of the gate.

Whereas, in the above-identified application, because a sidewall material covers most of the side surface of the gate, it is possible to maintain a high efficiency of the gate, etc., and to deter an escape of an impurity introduced into the gate electrode during manufacturing.

Applicants have added claims 13-16. In view of the aforementioned remarks, these claims are likewise distinguishable from the cited references and should be allowable.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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